Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Withdrawn) A method of operating a first-in first-out (FIFO) pointer circuit comprising:

coupling a plurality of shift registers in a circular fashion; and

applying a rising edge and a falling edge of a pointer clock signal to clock inputs of the plurality of shift registers in an alternating fashion.

2. (Withdrawn) A method of operating a first-in first-out (FIFO) pointer circuit comprising:

coupling a plurality of shift registers in a circular fashion;

applying the same one of a rising edge or a falling edge of a pointer clock signal to clock inputs of the plurality of shift registers in a full rate mode of operation; and

applying the rising edge and the falling edge of the pointer clock signal to clock inputs of the plurality of shift registers in an alternating fashion in a half rate mode of operation.

3. (Withdrawn) A first-in-first-out (FIFO) pointer reset circuit comprising:

a clock present detector coupled to receive a read clock and a write clock and configured to generate a CKPRES signal indicating status of the write clock; and

logic circuit coupled to receive a first reset signal, the CKPRES signal, the write clock and the read clock, and configured to generate a write pointer reset signal and a read pointer reset signal in response thereto.

4. (Withdrawn) The FIFO pointer reset circuit of claim 3 wherein the logic circuit further receives a lock detect signal indicating a phase status of the read clock, the lock detect signal being logically combined with other input signals to the logic circuit.

5. (Withdrawn) The FIFO pointer reset circuit of claim 3 wherein the logic circuit comprises:

a first flip-flop having a reset input coupled to receive a second reset signal, a clock input coupled to receive the read clock, and an output; and

a second flip-flop having a data input coupled to the output of the first flip-flop, a reset input coupled to receive the second reset signal, a clock input coupled to receive the read clock and an output coupled to generate the read pointer reset signal.

6. (Withdrawn) The FIFO pointer reset circuit of claim 5 wherein the logic circuit further comprises:

a third flip-flop having a reset input coupled to receive the second reset signal, a clock input coupled to receive the write clock, and an output; and

a fourth flip-flop having a data input coupled to the output of the third flip-flop, a reset input coupled to receive

the second reset signal, a clock input coupled to receive the write clock and an output coupled to generate the write pointer reset signal.

7. (Withdrawn) The FIFO pointer reset circuit of claim 6 wherein data input of the first flip-flop and a data input of the second flip-flop couple together and to a third reset signal.

8. (Withdrawn) The FIFO pointer reset circuit of claim 7 wherein the logic circuit further comprises a fifth flip-flop having a data input coupled to the first reset signal, a clock input coupled to the write clock, a reset input coupled to the second reset signal, and an output coupled to generate the third reset signal.

9. (Withdrawn) The FIFO pointer reset circuit of claim 6 wherein the logic circuit further comprises logic gates that combine the CKPRES signal with a lock detect signal that indicates a phase status of the read clock, and generate the second reset signal.

10. (Withdrawn) The FIFO pointer reset circuit of claim 6 further comprising a first multiplexer having a first input coupled to receive the read clock, a second input coupled to receive a second read clock having a frequency that is different than that of the read clock, a select input, and an output coupled to an input of the clock present detector, wherein a control signal applied to the select input selects one of either the read clock or the second read clock to be applied to the clock present detector.

11. (Withdrawn) The FIFO pointer reset circuit of claim 10 wherein the frequency of the second read clock is half that of the read clock.

12. (Withdrawn) The FIFO pointer reset circuit of claim 11 wherein the logic circuitry further comprises a second multiplexer having a first input coupled to the write clock, a second input coupled to an inverted version of the write clock, a select input, and an output coupled to the clock input of the third flip-flop.

13. (Withdrawn) The FIFO reset pointer circuit of claim 6 wherein the logic circuitry further comprises a selectable flip-flop that is selectably coupled in series with the first flip-flop, the selectable flip-flop having a reset input coupled to the second reset signal and a clock input coupled to receive the read clock.

14. (Withdrawn) A method of resetting first-in first-out (FIFO) pointer circuits comprising:

detecting the presence of a FIFO write clock signal and generating a CKPRES signal in response thereto;

detecting the lock status of a FIFO read clock signal phase-locked loop and generating a LCKDET signal in response thereto;

receiving a reset signal; and

logically combining the CKPRES, the LCKDET and the reset signal to reset the FIFO pointer circuits when the write clock signal is lost, or when the read clock is not locked, or when the reset signal is asserted.

15. (Withdrawn) The method of claim 14 wherein the step of logically combining further comprises resetting a pair of serially-coupled flip-flops that are clocked by the FIFO read clock.

16. (Original) A write clock present detector for a first-in first-out (FIFO) circuit, the write clock present detector comprising:

a read shift register having a first plurality of serially-coupled registers and configured to shift a read flag signal in response to a read clock;

a write shift register having a second plurality of serially-coupled registers and configured to shift a write flag signal in response to a write clock; and

a logic circuit coupled to an output of the read shift register and an output of the write shift register, and configured to logically combine the write flag signal with the read flag signal to generate a write clock present detect output signal.

17. (Original) The write clock present detector of claim 16 wherein the first plurality of registers in the read shift register is larger in number compared to the second plurality of registers in the write shift register.

18. (Original) The write clock present detector of claim 17 wherein the registers in the write shift register and the registers in the read shift register are resettable registers with each having a reset input.

19. (Original) The write clock present detector of claim 18 wherein the logic circuit comprises a reset circuit

having an input coupled to an output of the read shift register, and an output coupled to the reset input of each of the registers in the read and the write shift registers.

20. (Original) The write clock present detector of claim 19 wherein the reset circuit comprises a serially-coupled pair of flip-flops coupled to an output of the read shift register and a logic gate having inputs coupled to outputs of the pair of flip-flops and an output coupled to the output of the reset circuit.

21. (Original) The write clock present detector claim 17 wherein the write shift register comprises N registers and the read shift register comprises N+3 registers.

22. (Original) The write clock present detector of claim 21 wherein the logic circuit comprises:

a logic gate coupled to receive an output of the N^{th} write register and an output of the N^{th} read register and to generate a DET output signal; and

a flip-flop having a data input coupled to receive the DET output signal, a clock input coupled to the $(N+3)^{th}$ output of the read register, and an output coupled to generate a write clock present detect signal.

23. (Original) A method of detecting the presence of a write clock for a first-in first-out (FIFO) circuit, the method comprising:

propagating a read flag signal through a read shift register in response to a read clock;

propagating a write flag signal through a write shift register in response to the write clock; and

comparing an output of the read shift register with an output of the write shift register to generate a write clock present output signal.

24. (Original) The method of claim 23 further comprising periodically resetting the read shift register and the write shift register.

25. (Withdrawn) A first-in first-out (FIFO) pointer circuit comprising:

a serial chain of N registers coupled in circle and configured to shift a pointer signal in response to a pointer clock; and

a pointer abnormality detector having a logic circuit with N inputs respectively coupled to N outputs of the N registers,

wherein, the logic circuit is configured to detect lack of the pointer signal or presence of multiple pointer signals.

26. (Withdrawn) The FIFO pointer circuit of claim 25 wherein the logic circuit in the pointer abnormality detector comprises a first logic gate having N-1 inputs coupled to N-1 outputs of the N registers and an output, and a second logic gate having a first input coupled to the output of the first logic gate and a second input coupled to one output of the N registers that is not coupled to the first logic gate.

27. (Withdrawn) The FIFO pointer circuit of claim 26 wherein the logic circuit further comprises a flip-flop having a data input coupled to an output of the second logic gate, a clock input and an output.

28. (Withdrawn) The FIFO pointer circuit of claim 26 wherein the first logic gate is an OR gate, and the second logic gate is an exclusive NOR gate.

29. (New) The write clock present detector of claim 16 wherein the write clock present detect output signal is generated when the read and write flag signals propagate to the logic circuit.

30. (New) The write clock present detector of claim 16 comprising another shift register coupled to receive the output of the read shift register to generate a delayed read flag signal, wherein the logic circuit comprises:

a logic gate coupled to receive the output of the write shift register and the output of the read shift register; and

a register having a data input coupled to receive an output of the logic gate and having a clock input coupled to receive the delayed read flag signal to generate a write clock present signal.

31. (New) The method of claim 23 wherein the write clock present output signal is generated when the read and write flag signals propagate to a logic circuit.

32. (New) The method of claim 23 wherein the write clock present output signal is generated when the read and write flag signals propagate to a logic circuit before a reset occurs.

33. (New) The method of claim 23 comprising delaying the generation of the write clock present output signal after comparing the output of the read and write shift registers.

34. (New) The method of claim 23 comprising further propagating the read flag signal through the read shift register in response to the read clock to generate the write clock present output signal.

35. (New) The method of claim 23 comprising clocking a register with the further propagated read flag signal to generate the write clock present output signal.

36. (New) The method of claim 23 comprising using the read flag signal to generate a reset signal for the read and write shift registers.

37. (New) The method of claim 23 comprising further propagating the read flag signal through the read shift register in response to the read clock to generate a reset signal for the read and write shift registers.

38. (New) The method of claim 23 comprising initiating the propagation of the read flag signal and the write flag signal after generation of a reset signal for the read and write shift registers.